FEATURES

- Compatible with EIA-422 and TIA/EIA-485-A standard
- 2.5V~5.5V V_{CC1}, 4.5V~5.5V V_{CC2} power supply range, full-duplex
- Bus port ESD protection capacity of over 15kV HBM
- 1/8 unit load, allow up to 256 transceivers on the bus
- Driver Short-circuit protection, receiver open-circuit failure protection
- Low power shutdown function
- Data transmission up to 16Mbps in an electric noise environment
- Wide temperature range: -40℃~125℃
- Strong anti-noise ability
- High CMTI: ±100kV/μs (typical value)
- Up to 5000 VRMS isolation voltage resistance
- Isolation gate life: >40 years.
- Wide-body SOIC16 package, RoHS compliant

PRODUCT APPEARANCE

Provide green and environmentally friendly lead-free package

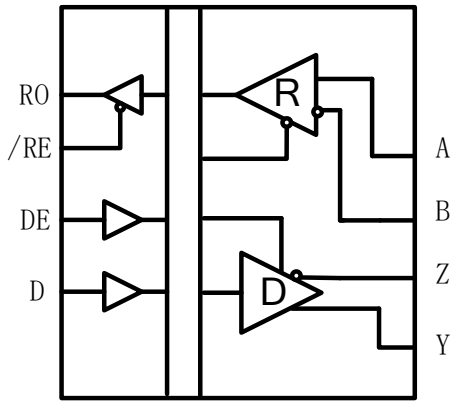
DESCRIPTION

The SIT3491ISO is a capacitive isolated full duplex RS-422/485 transceiver, and bus port ESD protection capacity of more than 15kV HBM. It is a RS-422/485 transceiver fully meet the requirements of TIA/EIA-422/485 standard.

The SIT3491ISO includes a driver and a receiver, both of which can be enabled and closed independently. When both are disabled, both the driver and the receiver output are high resistance state. SIT3491ISO has 1/8 load, which allows 256 SIT34991ISO transceivers to be connected to the same communication bus. It can realize error-free data transmission up to 16Mbps.

The SIT3491ISO has the functions of fail-safe, current-limiting protection, over-voltage protection, etc.

FUNCTIONAL SCHEMATIC BLOCK DIAGRAM



PIN CONFIGURATION

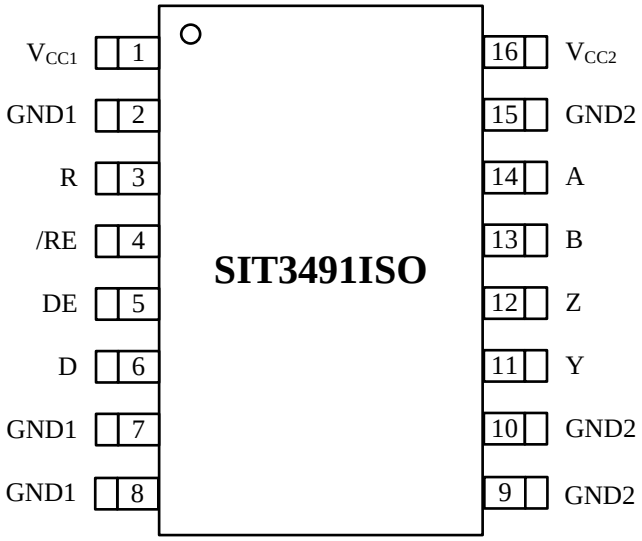


Fig 1 SIT3491ISO pin configuration

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	V_{CC1}	Power supply, V_{CC1}
2	GND1	Ground point of power supply V_{CC1}
3	R	Receiver Output. When /RE is low and if A - B≥-10mV, R will be high; if A - B≤-200mV, R will be low.

PIN	SYMBOL	DESCRIPTION
4	/RE	Receiver Output Enable. Drive /RE low to enable RO; RO is high impedance when /RE is high. Drive /RE high and DE low to enter low-power shutdown mode.
5	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive /RE high and DE low to enter low-power shutdown mode.
6	D	Driver Input。With DE high, a low on D forces non-inverting output low and inverting output high. Similarly, a high on D forces non-inverting output high and inverting output low.
7	GND1	Ground point of power supply V_{CC1}.
8	GND1	Ground point of power supply V_{CC1}.
9	GND2	Ground point of power supply V_{CC2}.
10	GND2	Ground point of power supply V_{CC2}.
11	Y	Non-inverting driver output
12	Z	Inverting driver output
13	B	Inverting receiver input
14	A	Non-inverting receiver input
15	GND2	Ground point of power supply V_{CC2}.
16	V_{CC2}	Power supply, V_{CC2}.

LIMITING VALUES

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage	V_{CC1}, V_{CC2}	-0.5~+6	V
control port voltage	/RE, DE, D	-0.5~V_{CC1}+0.5	V
Receiver output current	I_O	-10~+10	mA
Bus side input voltage	A, B, Z, Y	-15~+15	V
Virtual junction temperature	T_j	150	℃
Ambient temperature	T_{amb}	-40~125	℃
Storage temperature	T_{stg}	-65~150	℃

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

DRIVER DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Differential driver output (no load)	V_{OD1}		3.3		5.5	V
Differential driver output	V_{OD2}	Fig 2, RL = 54 Ω	1.5		VCC_2	V
		Fig 2, RL = 100 Ω	1.5		VCC_2	V
Change in magnitude of output voltage (NOTE1)	ΔV_{OD}	Fig 2, RL = 54 Ω			0.2	V
Common-mode output voltage	V_{OC}	Fig 2, RL = 54 Ω			3	V
Change in magnitude of common-mode output voltage (NOTE1)	ΔV_{OC}	Fig 2, RL = 54 Ω			0.2	V
Input high voltage	V_{IH}	D	2.0			V
Input low voltage	V_{IL}	D			0.8	V
Logic input current	I_{IN1}	D	-15		20	μA
Output short-circuit current (shorted to high)	I_{OSD1}	Shorted to 0V~12V	35		250	mA
Output short-circuit current (shorted to low)	I_{OSD2}	Shorted to -7V~0V	-250		-35	mA

(Unless otherwise noted, VCC_1 = 2.5V~5.5V, VCC_2 = 4.5V~5.5V, T_{amb}=-40~125℃, T_{amb}=25℃.)

NOTE1: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the D input changes state.

RECEIVER DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input current (A, B)	I_{IN2}	VCC_2=0 or 3.3V V_{IN} = 12 V			125	μA

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input current (A, B)	I_{IN2}	VCC_2=0 or 3.3V V_{IN} = -7 V	-200			μA
Positive input threshold voltage	V_{IT+}	-7V≤V_{CM}≤12V			-10	mV
Reverse input threshold voltage	V_{IT-}	-7V≤V_{CM}≤12V	-200			mV
Input hysteresis voltage	V_{hys}	-7V≤V_{CM}≤12V	10	30		mV
Output High voltage	V_{OH}	I_{OUT} = −4mA, V_{ID} = -10 mV	V_{CC2}-1.5			V
Output Low voltage	V_{OL}	I_{OUT} = +4mA, V_{ID} = -200 mV			0.4	V
Three-state leakage current	I_{OZR}	0.4V < V_O <2.4V			±15	μA
Receiver input resistance	R_{IN}	-7V≤V_{CM}≤12V	96			kΩ
Receiver short-circuit output current	I_{OSR}	0 V≤V_O≤VCC			±150	mA

(Unless otherwise noted, VCC_1 = 2.5V~5.5V, VCC_2 = 4.5V~5.5V, T_{amb}=-40~125℃, T_{amb}=25℃.)

SUPPLY CURRENT

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Current	I_{CC1}	V_{CC1}=5V /RE= DE=VCC, no load		3.2	4.16	mA
	I_{CC2}	V_{CC2}=5V /RE= DE=VCC, no load		2	2.6	mA

ESD PROTECTION

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
A, B, Y, Z		HBM		±15		kV
Other pots		HBM		±6		kV

DRIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Driver propagation delay, low-to-high level	t_{DPLH}	R_L = 54 Ω, C_L=100pF (Fig 3 & Fig 4)		15	35	ns
Driver propagation delay, high-to-low level	t_{DPHL}			15	35	ns
$\|t_{DPLH}-t_{DPHL}\|$	t_{SKEW1}			7	10	ns
Rising time/Falling time	t_{DR}, t_{DF}			10	25	ns
Output enable time to high level	t_{PZH}	R_L = 110Ω, (Fig 5 & Fig 6)	20		90	ns
Output enable time to low level	t_{PZL}		20		90	ns
Output disable time from low level	t_{PLZ}	R_L = 110Ω, (Fig 5 & Fig 6)	20		80	ns
Output disable time from high level	t_{PHZ}		20		80	ns
In Shutdown mode, Enable to output high	t_{DSH}	R_L = 110Ω, (Fig 5 & Fig 6)	500		900	ns
In Shutdown mode, Enable to output low	t_{DSL}	R_L = 110Ω, (Fig 5 & Fig 6)	500		900	ns

RECEIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Receiver propagation delay, low-to-high level	t_{RPLH}	V_{ID}≥2.0V; Rising and falling edge time V_{ID} ≤15ns (Fig 7 & Fig 8)	20	60	90	ns
Receiver propagation delay, high-to-low level	t_{RPHL}		20	60	90	ns
$\|t_{RPLH} - t_{RPHL}\|$	t_{SKEW2}			7	10	ns
Output enable time to low level	t_{RPZL}	C_L=15pF (Fig 7 & Fig 8)		20	50	ns

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output enable time to high level	t_{RPZH}	C_L=15pF (Fig 7 & Fig 8)		20	50	ns
Output disable time from low level	t_{RPLZ}	C_L=15pF (Fig 7 & Fig 8)		20	45	ns
Output disable time from high level	t_{RPHZ}	C_L=15pF (Fig 7 & Fig 8)		20	45	ns
In Shutdown mode, Enable to high level	t_{RPSH}	C_L=15pF (Fig 7 & Fig 8)		200	1400	ns
In Shutdown mode, Enable to output low	t_{RPSL}	C_L=15pF (Fig 7 & Fig 8)		200	1400	ns
Time to Shutdown	t_{SHDN}	NOTE2	80		300	ns

NOTE2: If the enable inputs are RE=high and DE=low for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 300ns, the device is guaranteed to have entered shutdown.

FUNCTION TABLE

Transmitter function truth table

V_{CC1}	V_{CC2}	INPUT	ENABLE INPUT	OUTPUTS	
		(DI)	(DE)	Y	Z
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Z	Z
PU	PU	X	OPEN	Z	Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Z	Z
PU	PD	X	X	Z	Z
PD	PD	X	X	Z	Z

(1) PU = Power up; PD =Power down; H =High level; L=Low level; X = Irrelevant; Z =High impedance.

Receiver function truth table

V_{CC1}	V_{CC2}	Differential Input $V_{ID}=(V_A-V_B)$	Enable (/RE)	Output (R)
PU	PU	$-0.01V \le V_{ID}$	L/OPEN	H
PU	PU	$-0.2V < V_{ID} < -0.01V$	L/OPEN	?
PU	PU	$V_{ID} \le -0.2V$	L/OPEN	L
PU	PU	X	H	Z
PU	PU	Open circuit	L	H
PU	PU	Short circuit	L	H
PU	PU	idle	L	H
PD	PU	X	X	Z
PU	PD	X	X	H
PD	PD	X	X	Z

(1) PU=Power up; PD=Power down; H=High level; L=Low level; X=Irrelevant; Z=High impedance; ? = Uncertain.

TEST CIRCUIT

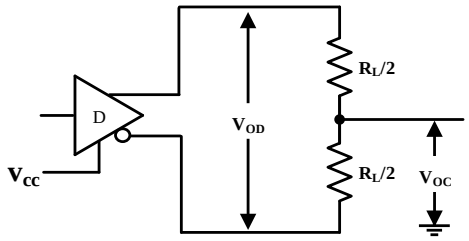
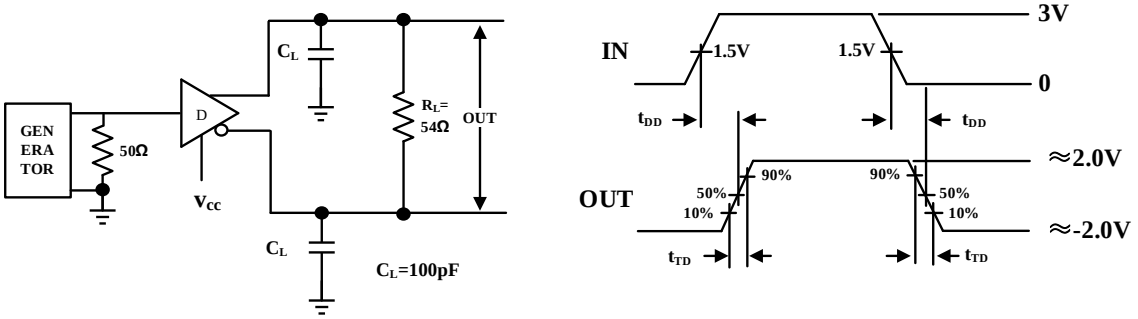


Fig 2 Driver DC test load



CL includes probe and stray capacitance (the same below).

Fig 3 Differential delay and transit time of driver

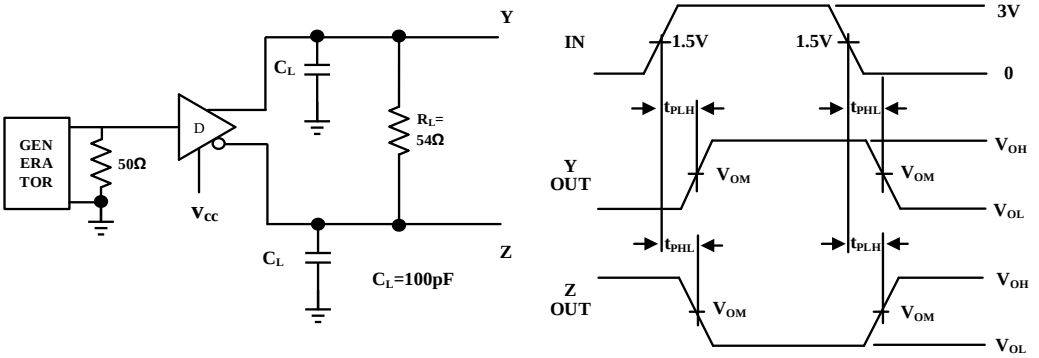


Fig 4 Drive propagation delay

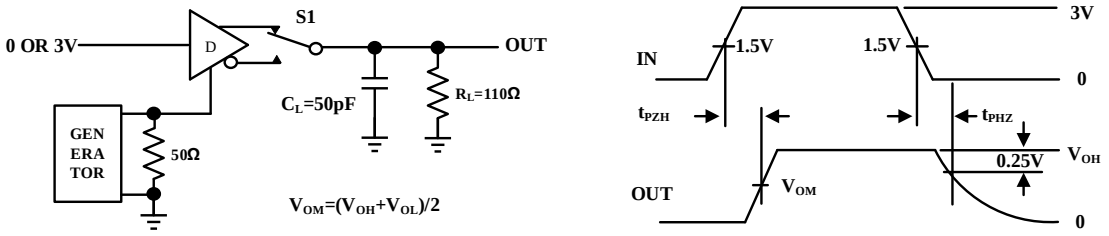


Fig 5 Drive enable and disable time

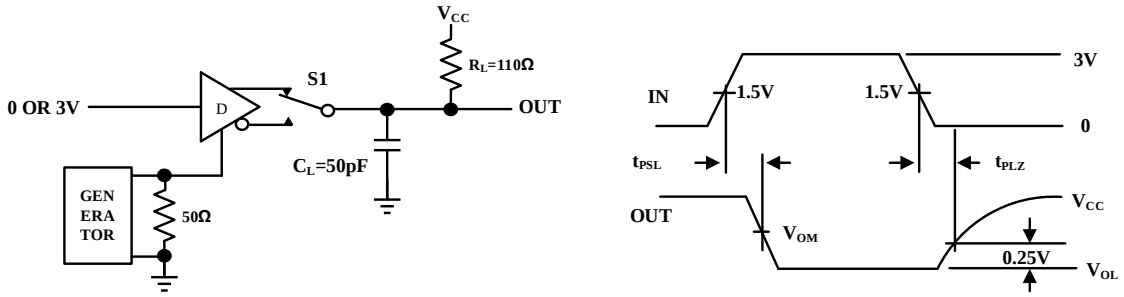


Fig 6 Drive enable and disable time

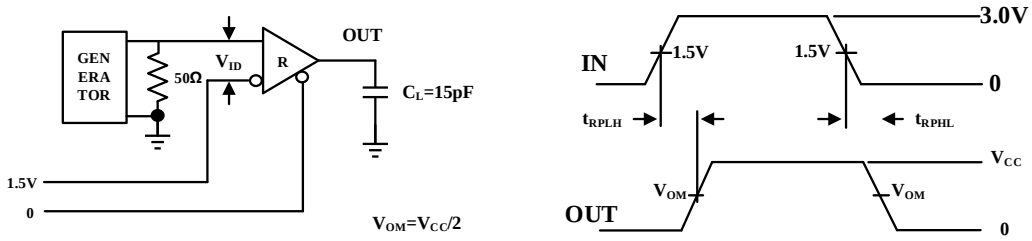
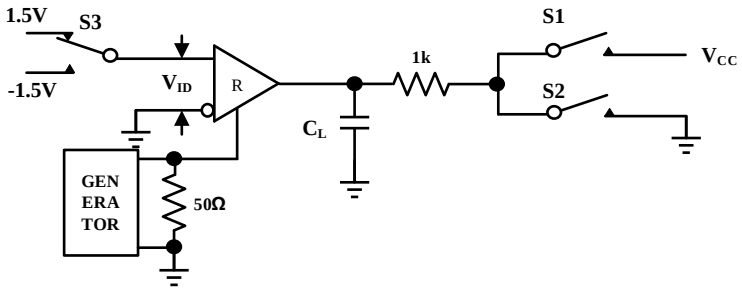


Fig 7 Receiver propagation delay test circuit



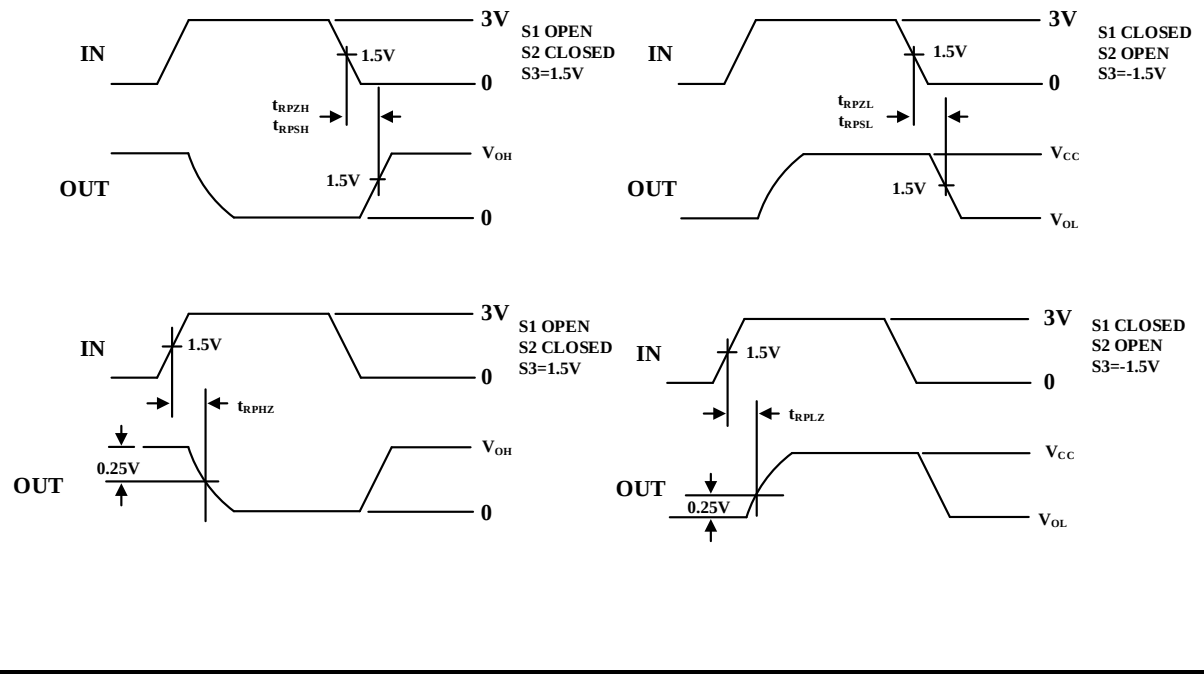


Fig 8 Receiver enable and disable time

ADDITIONAL DESCRIPTION

1 Sketch

The SIT34991ISO is a capacitive isolated full duplex RS-422/RS-485 transceiver, and bus port ESD protection capacity of more than 15kV HBM, including a driver and receiver. It has the functions of fail-safe, over-voltage protection, and over-current protection. SIT3491ISO realizes error-free data transmission up to 16Mbps.

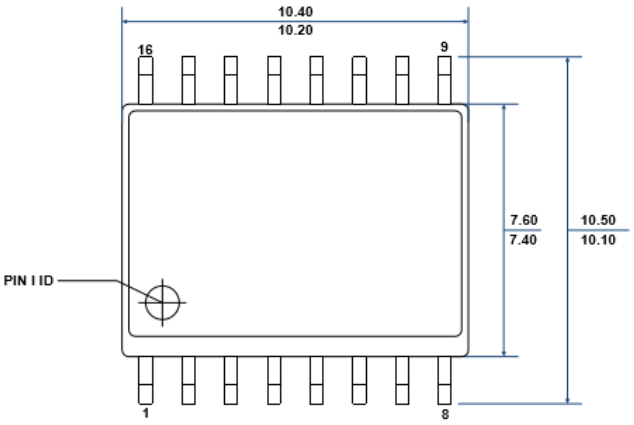
2 Allowing up to 256 transceivers on the Bus

The input impedance of the standard RS485 receiver is 12kΩ (1 unit load), and the standard driver can drive up to 32 unit loads. The receiver of SIT3491ISO transceiver has 1/8 unit load input impedance (96kΩ), which allows up to 256 transceivers to be connected on the same communication bus in parallel. These devices can be combined arbitrarily or with other RS485 transceivers. Any combination of these devices and/or other RS485 transceivers with a total of 32 unit loads or less can be connected to the line.

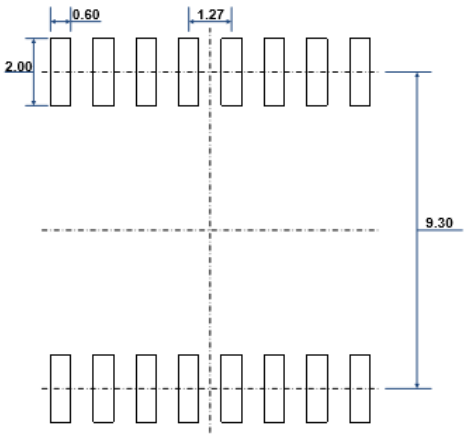
3 Driver output protection

Over-current and overvoltage protection mechanisms are used to prevent excessive output current and power dissipation caused by faults or bus contention, providing fast short circuit protection over the entire common mode voltage range(refer to typical operating characteristics).

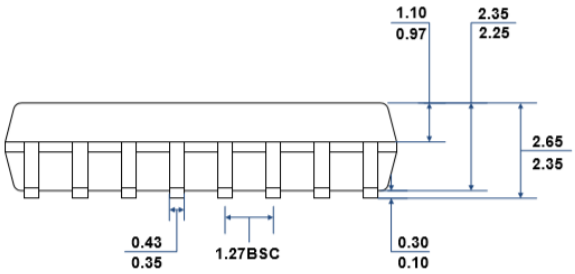
SOIC16-WB WIDE BODY DIMENSIONS



TOP VIEW



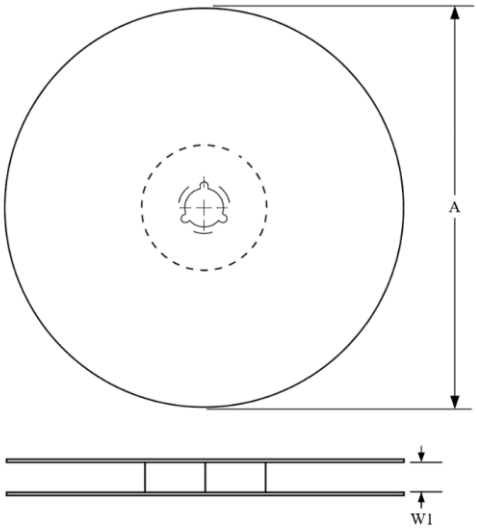
LAND PATTERN EXAMPLE (Unit: mm)



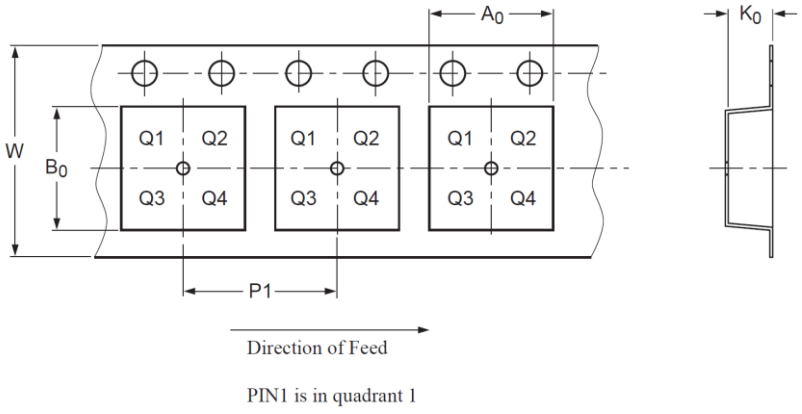
FRONT VIEW

SIDE VIEW

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

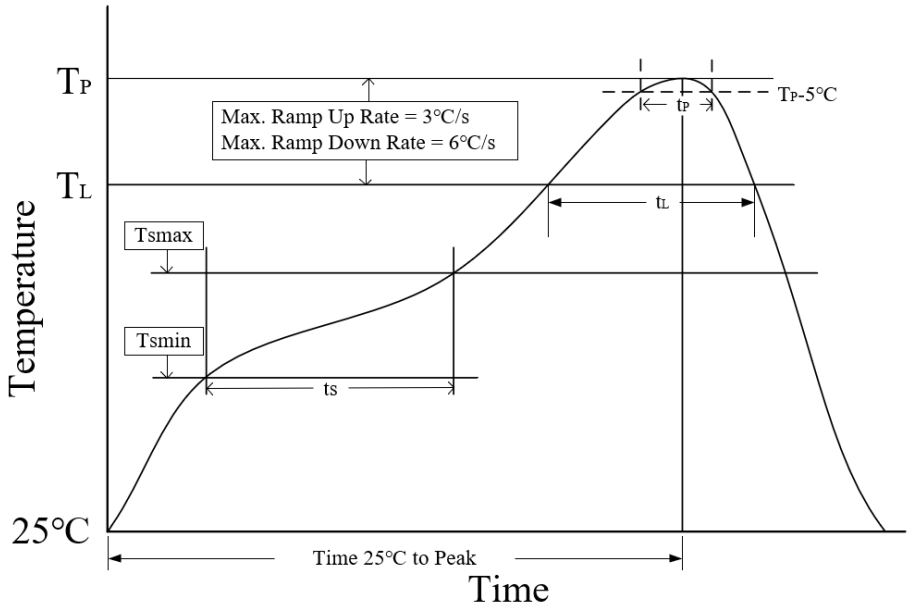
Package type	Reel diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOPW16	330±2.0	$16.4^{+2.0}_{+0.0}$	10.75±0.1	10.70±0.10	2.80±0.10	12.00±0.10	16.00±0.20

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SIT3491ISO	SOPW16, body wide SOP16	Tape and reel

SOPW16 is packed with 1000 pieces/disc in braided packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L)T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision Date
V1.0~V1.1	Product datasheet.	November 2020
V1.2	Updated I_{IN1} parameters; Updated test condition of electrical parameters; Updated I_{IN2} parameters; Updated I_{OSR} parameters and test condition; Adjusted format.	October 2021
V1.3	Deleted overtemperature information; Added ambient temperature range T_{amb}; Updated V_{OD2} parameters; Updated V_{OD2}, ΔV_{OD}, V_{OC}; ΔV_{OC} test condition; Updated test circuit; Added tape and reel information; Updated ordering information; Added reflow soldering information; Added important statement; Added revision history.	July 2023